

1M-BIT CMOS STATIC RAM**128K-WORD BY 8-BIT****Description**

The μ PD431000A is a high speed, low power, and 1,048,576 bits (131,072 words $\times$ 8 bits) CMOS static RAM.

The μ PD431000A has two chip enable pins ($\overline{\text{CE1}}$, CE2) to extend the capacity. And battery backup is available. In addition to this, B version is a wide voltage version.

The μ PD431000A is packed in 32-pin plastic DIP, 32-pin plastic SOP, and 32-pin plastic TSOP(I).

Features

- 131,072 words by 8 bits organization
- Fast access time: 70, 85, 100, 150 ns (MAX.)
- Wide voltage range: B version
- 2 V (MIN.) data retention
- Output Enable input for easy application
- Two Chip Enable inputs: $\overline{\text{CE1}}$, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Standby supply current μ A (MAX.)	Data retention supply current ^{Note 1} μ A (MAX.)
μ PD431000A-L	70, 85	4.5 to 5.5	0 to 70	100	15
μ PD431000A-LL				50	3
μ PD431000A-B15	100 ^{Note 2} , 150	2.2 to 5.5		25 ^{Note 3}	

Notes 1. $T_A \leq 40^\circ\text{C}$

2. $V_{CC} = 4.5$ to 5.5 V

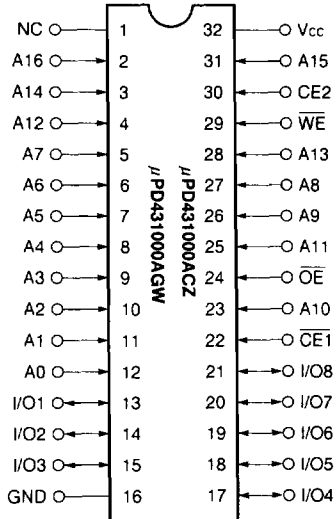
3. $50\ \mu\text{A}$ ($V_{CC} > 3.3$ V)

Ordering Information

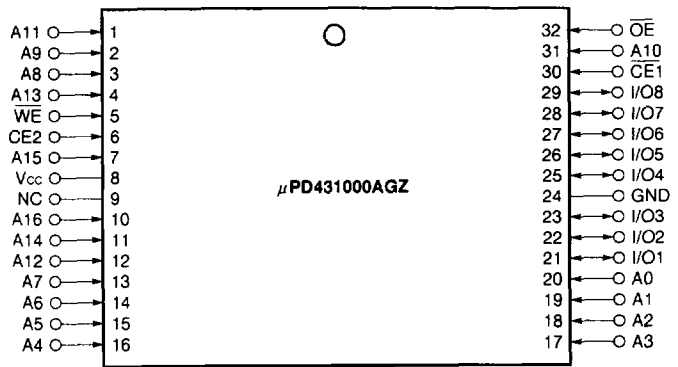
Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μ PD431000ACZ-70L	32-pin Plastic DIP (600 mil)	70	4.5 to 5.5	0 to 70	L Version
μ PD431000ACZ-85L		85			LL Version
μ PD431000ACZ-70LL		70			
μ PD431000ACZ-85LL		85			L Version
μ PD431000AGW-70L	32-pin Plastic SOP (525 mil)	70			LL Version
μ PD431000AGW-85L		85			
μ PD431000AGW-70LL		70			B Version
μ PD431000AGW-85LL		85			LL Version
μ PD431000AGW-B15	32-pin Plastic TSOP (I) (8 × 20 mm)	150	2.2 to 5.5		B Version
μ PD431000AGZ-70LL		70	4.5 to 5.5		LL Version
μ PD431000AGZ-B15		150	2.2 to 5.5		B Version

Pin Configuration (Marking side)

32-pin Plastic DIP (600 mil)
32-pin Plastic SOP (525 mil)

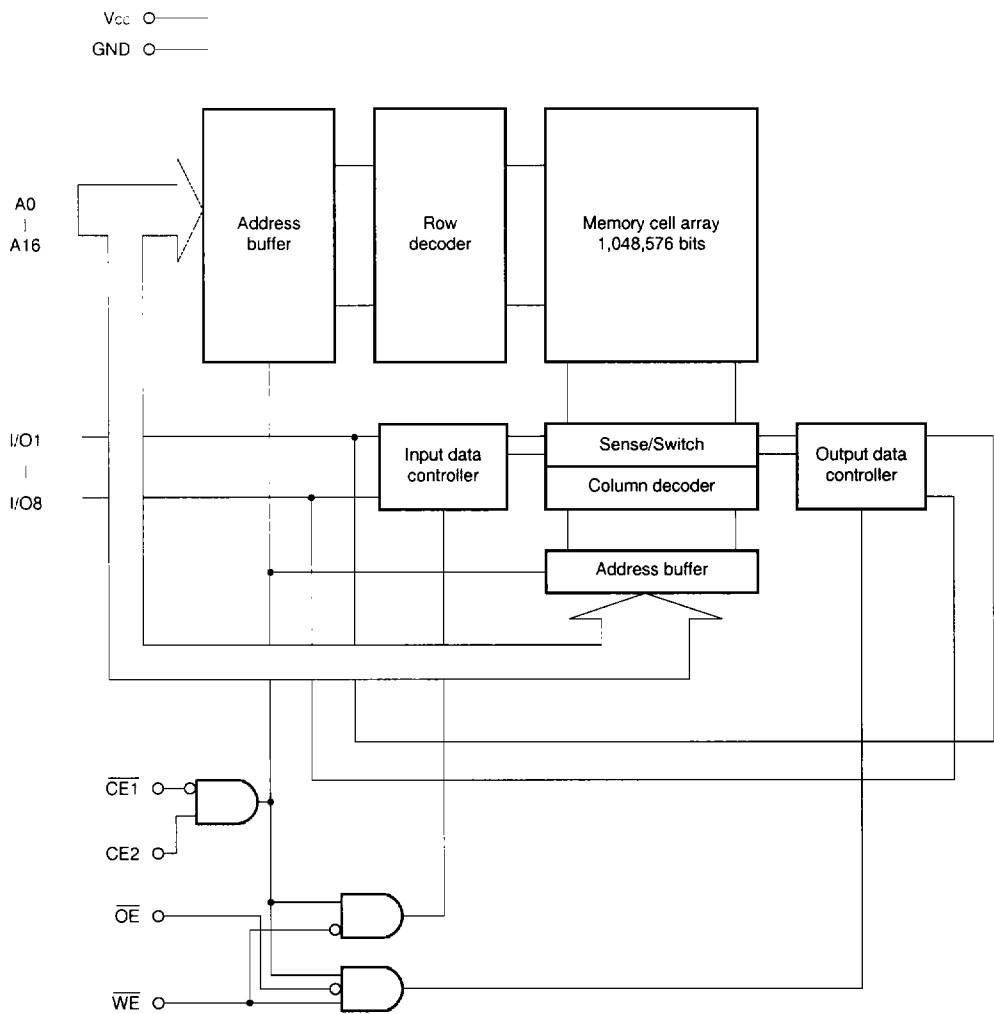


32-pin Plastic TSOP (I) (8 × 20mm)



A0 to A16 : Address inputs
I/O1 to I/O8 : Data inputs/outputs
CE1, CE2 : Chip Enable 1, 2
WE : Write Enable
OE : Output Enable
Vcc : Power supply
GND : Ground
NC : No connection

Block Diagram



Truth Table

$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O	Supply current
H	x	x	x	Not selected	High impedance	I _{ss}
x	L	x	x			I _{CCA}
L	H	H	H	Output disable		
L	H	L	H	Read	D _{OUT}	
L	H	x	L	Write	D _{IN}	

Remark x : Don't care

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 ^{Note} to +7.0	V
Input/Output voltage	V _I	-0.5 ^{Note} to V _{CC} + 0.5	V
Operating ambient temperature	T _A	0 to 70	°C
Storage temperature	T _{stg}	-55 to +125	°C

Note -3.0 V (MIN.) (Pulse width 30 ns)

Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	μPD431000A-L μPD431000A-LL		μPD431000A-B15		Unit
		MIN.	MAX.	MIN.	MAX.	
Supply voltage	V _{CC}	4.5	5.5	2.2	5.5	V
High level input voltage	V _{IH}	2.2	V _{CC} + 0.5	2.2	V _{CC} + 0.5	V
Low level input voltage	V _{IL}	-0.3 ^{Note}	+0.8	-0.3 ^{Note}	+0.5	V
Operating ambient temperature	T _A	0	70	0	70	°C

Note -3.0 V (MIN.) (Pulse width 30 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	μ PD431000A-L			μ PD431000A-LL			μ PD431000A-B15			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	$V_{IN} = 0 \text{ V to } V_{CC}$	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{IO} = 0 \text{ V to } V_{CC}$, $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
Operating supply current	I_{CCA1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$ Minimum cycle time $I_{IO} = 0 \text{ mA}$		40	70		40	70			70	mA
		$V_{CC} \leq 3.3 \text{ V}$			—			—			20	
	I_{CCA2}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $I_{IO} = 0 \text{ mA}$			15			15			15	
		$V_{CC} \leq 3.3 \text{ V}$			—			—			5	
	I_{CCA3}	$\overline{CE1} \leq 0.2 \text{ V}$, $CE2 \geq V_{CC} - 0.2 \text{ V}$, Cycle = 1 MHz, $I_{IO} = 0 \text{ mA}$, $V_{IL} \leq 0.2 \text{ V}$, $V_{IH} \geq V_{CC} - 0.2 \text{ V}$			10			10			10	
		$V_{CC} \leq 3.3 \text{ V}$			—			—			5	
Standby supply current	I_{SB}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$			3			3			3	mA
		$V_{CC} \leq 3.3 \text{ V}$			—			—			2	
	I_{SB1}	$\overline{CE1} \geq V_{CC} - 0.2 \text{ V}$, $CE2 \geq V_{CC} - 0.2 \text{ V}$		2	100		1	50		1	50	μA
		$V_{CC} \leq 3.3 \text{ V}$			—			—		0.5	25	
	I_{SB2}	$CE2 \leq 0.2 \text{ V}$		2	100		1	50		1	50	
		$V_{CC} \leq 3.3 \text{ V}$		—	—		—	—		0.5	25	
High level output voltage	V_{OH1}	$I_{OH} = -1.0 \text{ mA}$, $V_{CC} \geq 4.5 \text{ V}$	2.4			2.4			2.4			V
		$I_{OH} = -0.5 \text{ mA}$	—			—			2.4			
	V_{OH2}	$I_{OH} = -0.02 \text{ mA}$	—			—			$V_{CC} - 0.1$			
Low level output voltage	V_{OL1}	$I_{OL} = 2.1 \text{ mA}$, $V_{CC} \geq 4.5 \text{ V}$			0.4			0.4			0.4	V
		$I_{OL} = 1.0 \text{ mA}$			—			—			0.4	
	V_{OL2}	$I_{OL} = 0.02 \text{ mA}$			—			—			0.1	

Remark These DC characteristics are in common regardless of package types and access time.

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0 \text{ V}$			6	pF
Input/Output capacitance	C_{IO}	$V_{IO} = 0 \text{ V}$			10	pF

Remarks 1. V_{IN} : Input voltage

2. These parameters are periodically sampled and not 100 % tested.

Read Cycle

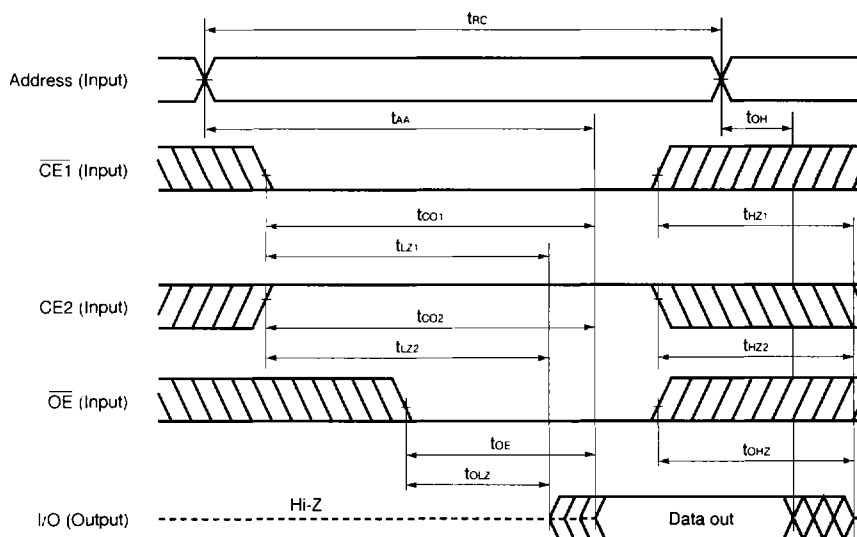
Parameter	Symbol	V _{CC} ≥ 4.5 V						V _{CC} ≥ 2.2 V		Unit	Condition
		μPD431000A-70		μPD431000A-85		μPD431000A-B15		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	70		85		100		150		ns	
Address access time	t _{AA}		70		85		100		150	ns	Note 1
$\overline{\text{CE1}}$ access time	t _{CO1}		70		85		100		150	ns	
CE2 access time	t _{CO2}		70		85		100		150	ns	
$\overline{\text{OE}}$ to output valid	t _{OE}		35		45		50		70	ns	
Output hold from address change	t _{OH}	10		10		10		10		ns	
$\overline{\text{CE1}}$ to output in low impedance	t _{LZ1}	10		10		10		10		ns	Note 2
CE2 to output in low impedance	t _{LZ2}	10		10		10		10		ns	
$\overline{\text{OE}}$ to output in low impedance	t _{OLZ}	5		5		5		5		ns	
$\overline{\text{CE1}}$ to output in high impedance	t _{HZ1}		25		30		35		50	ns	
CE2 to output in high impedance	t _{HZ2}		25		30		35		50	ns	
$\overline{\text{OE}}$ to output in high impedance	t _{OHZ}		25		30		35		50	ns	

Notes 1. See the output load shown in **Figure 1** except for μ PD431000A-B15.

2. See the output load shown in **Figure 2** except for μ PD431000A-B15.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Read Cycle Timing Chart



Remark In read cycle, $\overline{\text{WE}}$ should be fixed to high level.

AC Characteristics (Recommended operating conditions unless otherwise noted)

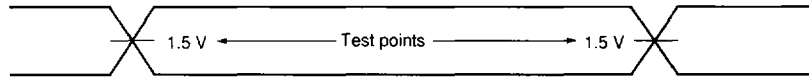
AC Test Conditions

Input waveform (Rise/fall time ≤ 5 ns)

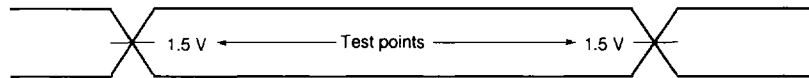
Input pulse levels

0.8 V to 2.2 V : μPD431000A-L, μPD431000A-LL

0.5 V to 2.2 V : μPD431000A-B15



Output waveform



Output load

μPD431000A-B15 : 1TTL + 100 pF

μPD431000A-L, 431000A-LL:

AC characteristics with notes should be measured with the output load shown in

Figure 1 and **Figure 2**.

Figure 1

(For t_{AA} , t_{CO1} , t_{CO2} , t_{OE} , t_{OH})

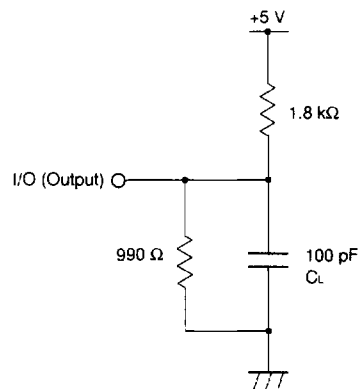
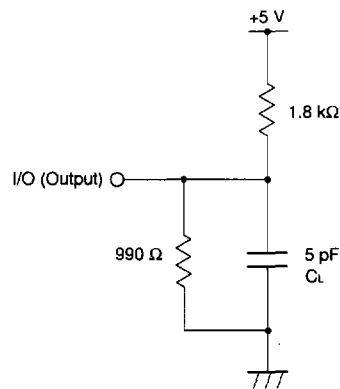


Figure 2

(For t_{LZ1} , t_{LZ2} , t_{OLZ} , t_{HZ1} , t_{HZ2} , t_{OHZ} , t_{WHZ} , t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

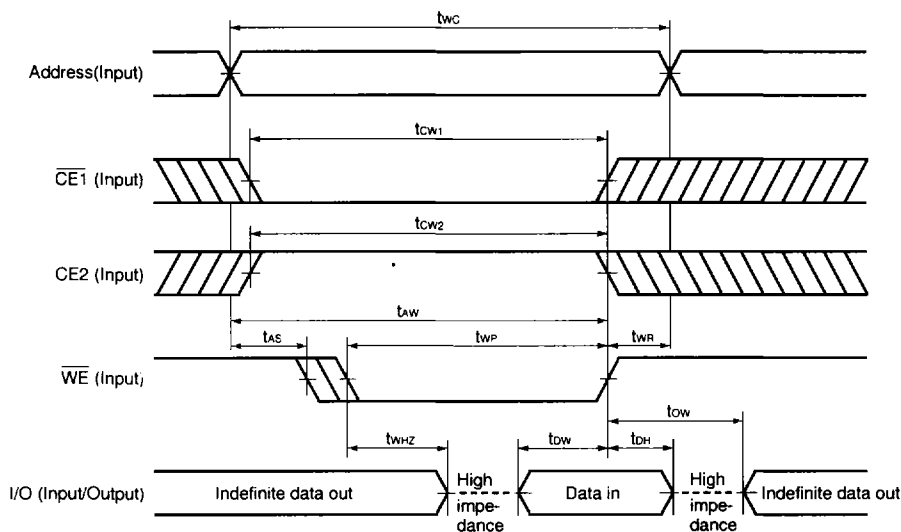
Write Cycle

Parameter	Symbol	Vcc ≥ 4.5 V						Vcc ≥ 2.2 V		Unit	Condition
		μPD431000A-70		μPD431000A-85		μPD431000A-B15		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	70		85		100		150		ns	
$\overline{\text{CE1}}$ to end of write	t _{CW1}	55		70		85		120		ns	
CE2 to end of write	t _{CW2}	55		70		85		120		ns	
Address valid to end of write	t _{AW}	55		70		85		120		ns	
Address setup time	t _{AS}	0		0		0		0		ns	
Write pulse width	t _{WP}	50		60		70		100		ns	
Write recovery time	t _{WR}	5		5		5		10		ns	
Data valid to end of write	t _{DW}	35		35		40		80		ns	
Data hold time	t _{DH}	0		0		0		0		ns	
$\overline{\text{WE}}$ to output in high impedance	t _{WHZ}		25		30		35		50	ns	Note
Output active from end of write	t _{OW}	5		5		5		5		ns	

Note See the output load shown in **Figure 2** except for μ PD431000A-B15.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

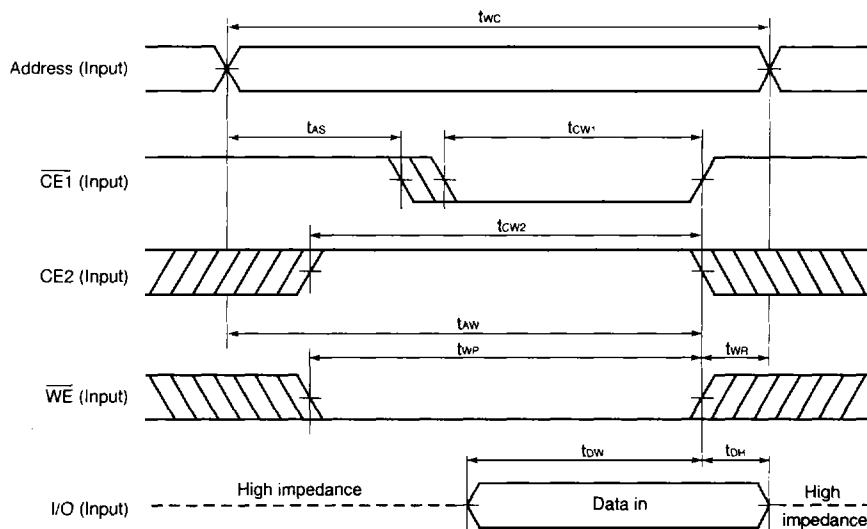
Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)



- Cautions**
1. During address transition, at least one of pins $\overline{CE1}$, $CE2$, $\overline{WE}$ should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

- Remarks**
1. Write operation is done during the overlap time of a low level $\overline{CE1}$, $\overline{WE}$, and a high level $CE2$.
 2. If $\overline{CE1}$ changes to low level at the same time or after the change of $\overline{WE}$ to low level, or if $CE2$ changes to high level at the same time or after the change of $\overline{WE}$ to low level, the I/O pins will remain high impedance state.
 3. When $\overline{WE}$ is at low level, the I/O pins are always high impedance. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the I/O pins high impedance.

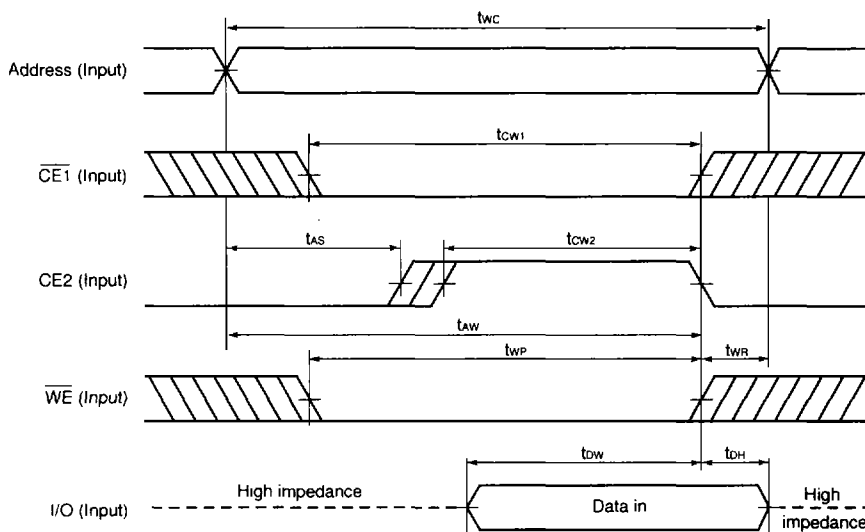
Write Cycle Timing Chart 2 ($\overline{\text{CE1}}$ Controlled)



- Cautions**
1. During address transition, at least one of pins $\overline{\text{CE1}}$, CE2 , $\overline{\text{WE}}$ should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level $\overline{\text{CE1}}$, $\overline{\text{WE}}$, and a high level CE2 .

Write Cycle Timing Chart 3 (CE2 Controlled)



- Cautions**
1. During address transition, at least one of pins $\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$ should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level $\overline{CE1}$, $\overline{WE}$, and a high level CE2.

Low V_{CC} Data Retention Characteristics

L Version (μPD431000A-L: T_A = 0 to 70 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{CCDR1}	$\overline{CE1} \geq V_{CC} - 0.2 \text{ V}, CE2 \geq V_{CC} - 0.2 \text{ V}$	2.0		5.5	V
	V _{CCDR2}	$CE2 \leq 0.2 \text{ V}$	2.0		5.5	
Data retention supply current	I _{CCDR1}	$V_{CC} = 3.0 \text{ V}, \overline{CE1} \geq V_{CC} - 0.2 \text{ V},$ $CE2 \geq V_{CC} - 0.2 \text{ V or } CE2 \leq 0.2 \text{ V}$		1	50 ^{Note}	μA
	I _{CCDR2}	$V_{CC} = 3.0 \text{ V}, CE2 \leq 0.2 \text{ V}$		1	50 ^{Note}	
Chip deselection to data retention mode	t _{CDR}		0			ns
Operation recovery time	t _R		5			ms

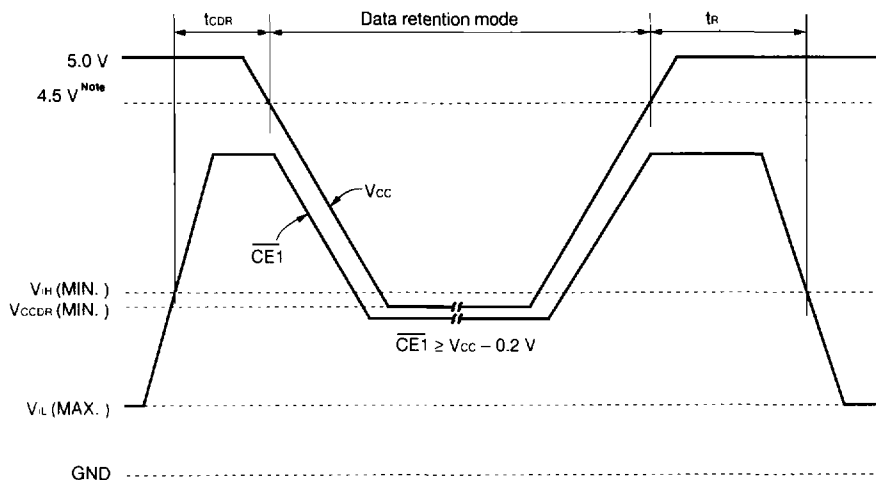
Note 15 μA (T_A ≤ 40 °C)

LL Version and B Version (μPD431000A-LL, 431000A-B: T_A = 0 to 70 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{CCDR1}	$\overline{CE1} \geq V_{CC} - 0.2 \text{ V}, CE2 \geq V_{CC} - 0.2 \text{ V}$	2.0		5.5	V
	V _{CCDR2}	$CE2 \leq 0.2 \text{ V}$	2.0		5.5	
Data retention supply current	I _{CCDR1}	$V_{CC} = 3.0 \text{ V}, \overline{CE1} \geq V_{CC} - 0.2 \text{ V},$ $CE2 \geq V_{CC} - 0.2 \text{ V or } CE2 \leq 0.2 \text{ V}$		0.5	20 ^{Note}	μA
	I _{CCDR2}	$V_{CC} = 3.0 \text{ V}, CE2 \leq 0.2 \text{ V}$		0.5	20 ^{Note}	
Chip deselection to data retention mode	t _{CDR}		0			ns
Operation recovery time	t _R		5			ms

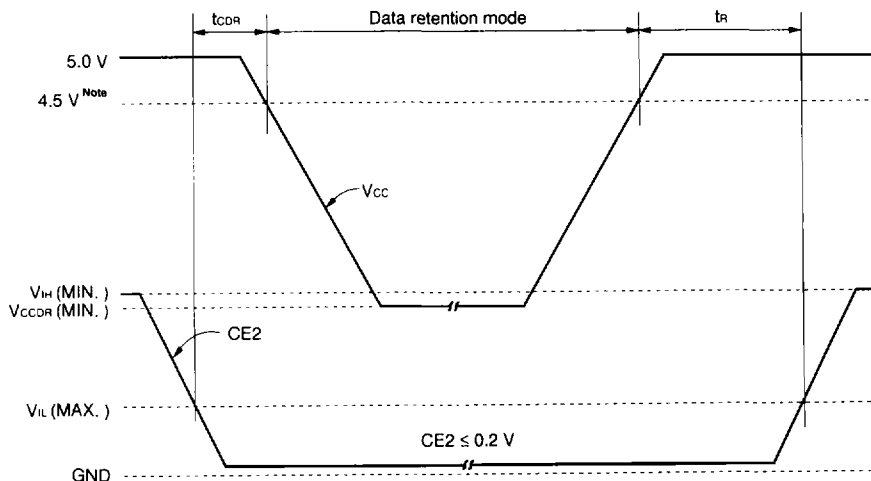
Note 3 μA (T_A ≤ 40 °C)

Data Retention Timing Chart

(1) $\overline{\text{CE1}}$ Controlled

Note B version : 2.2 V

Remark On the data retention mode by controlling $\overline{\text{CE1}}$, the input level of CE2 must be $\text{CE2} \geq V_{CC} - 0.2 \text{ V}$ or $\text{CE2} \leq 0.2 \text{ V}$. The other pins (Address, I/O, $\overline{\text{WE}}$, $\overline{\text{OE}}$) can be in high impedance state.

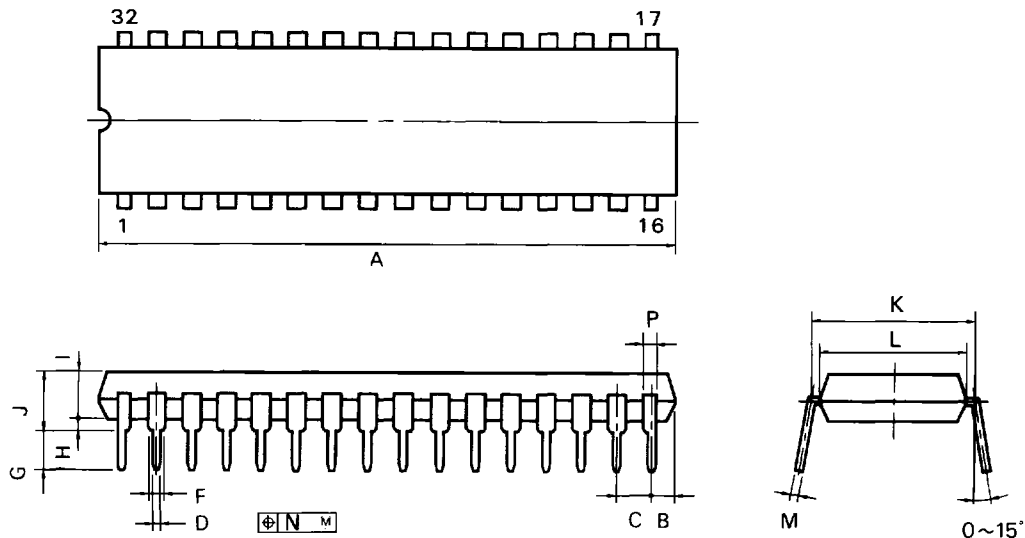
(2) CE2 Controlled

Note B version : 2.2 V

Remark The other pins ($\overline{\text{CE1}}$, Address, I/O, $\overline{\text{WE}}$, $\overline{\text{OE}}$) can be in high impedance state.

Package Drawings

32PIN PLASTIC DIP (600 mil)



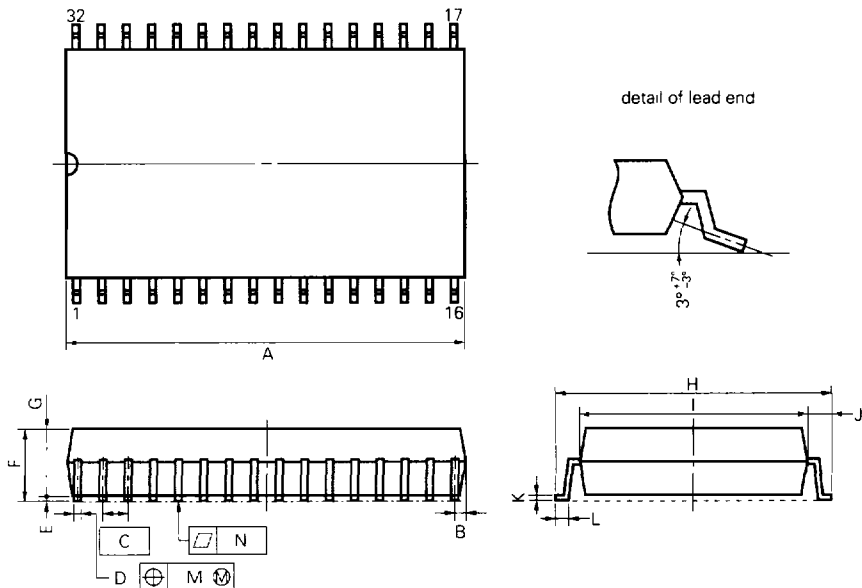
P32C-100-600A

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	40.64 MAX.	1.600 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ^{0.10}	0.020 ^{0.004} _{0.005}
F	1.1 MIN.	0.043 MIN.
G	3.2 ^{0.3}	0.126 ^{0.012}
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 ^{0.10} _{0.05}	0.010 ^{0.004} _{0.003}
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

32 PIN PLASTIC SOP (525 mil)



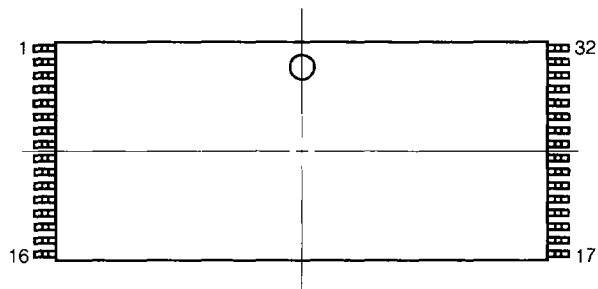
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

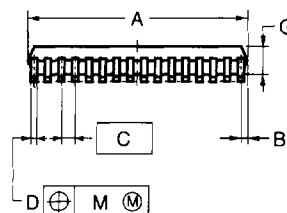
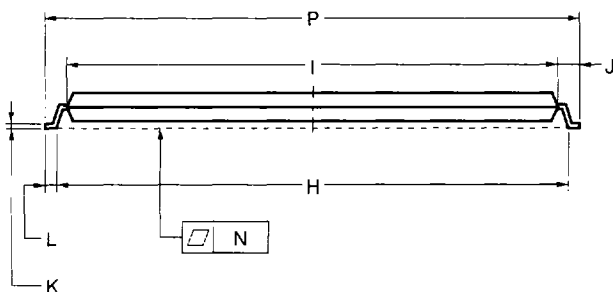
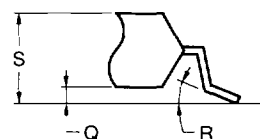
P32GW-50-525A

ITEM	MILLIMETERS	INCHES
A	20.61 MAX.	0.812 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.05}	0.016 ^{+0.004} _{-0.003}
E	0.15±0.05	0.006
F	2.95 MAX.	0.117 MAX.
G	2.7	0.106
H	14.1±0.3	0.555±0.012
I	11.3	0.445
J	1.4±0.2	0.055±0.008
K	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.12	0.005
N	0.10	0.004

32 PIN PLASTIC TSOP (I) (8×20)



detail of lead end



NOTES

- (1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.
- (2) "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX. < 0.327 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	8.0±0.1	0.315±0.004
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	19.0±0.2	0.748±0.008
I	18.4±0.2	0.724 ^{+0.009} _{-0.008}
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.125 ^{+0.10} _{-0.05}	0.005 ^{+0.004} _{-0.002}
L	0.5±0.1	0.020 ^{+0.004} _{-0.005}
M	0.08	0.003
N	0.10	0.004
P	20.0±0.2	0.787 ^{+0.009} _{-0.008}
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.1 MAX.	0.044 MAX.

S32GZ-50-KJH-3

[MEMO]

Recommended Soldering Conditions

The following conditions must be met when soldering the μ PD431000A.

For more details, refer to our document “**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL**” (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μ PD431000AGW: 32-pin Plastic SOP (525 mil)

μ PD431000AGZ: 32-pin Plastic TSOP(I) (8 × 20 mm)

Please consult with our sales offices

Type of Through Hole Mount Device

μ PD431000ACZ: 32-pin Plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature: 300 °C or below, Time: 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.